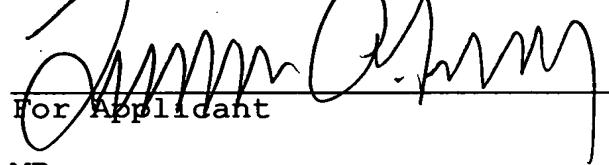


paragraph on page 5 makes it clear that the control gate of the EPROM may be formed of the second silicon layer. Figures 4 and 5 have been amended in accordance with the changes in the specification to better illustrate the memory cell.

In view of the foregoing, reconsideration and allowance of claims 1-10 are solicited.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Herbert L. Lerner, No. 12-1099.

Respectfully submitted,



For Applicant

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